CLAIMS

What is claimed is:

1. An integrated circuit (IC), including circuitry arranged in an array having a plurality of rows and a plurality of columns, wherein each row of the plurality of rows begins at a first side of the IC and ends at a second side of the IC, and each column of the plurality of columns begins at a third side of the IC and ends at a fourth side of the IC, the IC comprising:

a column of the plurality of columns comprising a plurality of circuit elements of a circuit type substantially occupying the column; and

a row of the plurality of rows positioned at the third side of the IC, wherein a number of circuit elements of an input and output circuit type in the row is less than a number of remaining circuit elements of other circuit types in the row.

2. The integrated circuit of claim 1 wherein the circuit type is selected from a group consisting of a Configurable Logic Block (CLB) type, a Multi-Giga Bit Transceiver (MGT) type, a Block Random Access Memory (BRAM) type, a Digital Signal Processor (DSP) circuit type, a multiplier circuit type, an arithmetic circuit type, an Input/Output Interconnect (IOI) circuit type, an Input/Output Block (IOB) type, and an application specific circuit type.

3. The integrated circuit of claim 1 wherein the input and output circuit type is an Input/Output Block (IOB) type.

4. The integrated circuit of claim 1 wherein the input and output circuit type includes an Input/Output Block type and a Multi-Giga Bit Transceiver type.

5. The integrated circuit of claim 1 further comprising a center column comprising configuration logic.

6. The integrated circuit of claim 3 wherein the center column is positioned on or near the center axis of the IC.

7. The integrated circuit of claim 4 further comprising a clock column adjacent to the center column.

8. The integrated circuit of claim 1 wherein the column of the plurality of columns further comprises a spacer tile and a clock tile.

9. The integrated circuit of claim 1 further comprising an embedded processor.

10. An integrated circuit (IC) comprising circuitry having programmable functions and programmable interconnects, the IC further comprising:

a plurality of homogeneous columns and

wherein each of the homogeneous columns starts at one side of the IC and ends at an opposite side of the IC, and

wherein a first column of the plurality of homogeneous columns comprises a first set of substantially identical circuit elements of a first circuit type substantially filling the first column.

11. The integrated circuit of claim 10:

wherein a second column of the plurality of homogeneous columns comprises a second set of substantially identical circuit elements of a second circuit type substantially filling the second column, and

wherein a third column of the plurality of homogeneous columns comprises a third set of substantially identical circuit elements of a third circuit type substantially filling the third column.

12. The integrated circuit of claim 10 further comprising a heterogeneous center column having configuration logic, a clock management circuit element, and an input/output block.

13. The integrated circuit of claim 10 wherein the first circuit type is selected from a group consisting of a Configurable Logic Block (CLB) type, a Multi-Giga Bit Transceiver (MGT) type, a Block Random Access Memory (BRAM) type, a fixed logic type, an Input/Output Interconnect (IOI) circuit type, and an Input/Output Block (IOB) type.

14. The integrated circuit of claim 13 wherein the fixed logic type comprises a Digital Signal Processor (DSP) circuit type, a multiplier circuit type, an arithmetic circuit type, and an application specific circuit type.

15. The integrated circuit (IC) of claim 10 wherein the integrated circuit further comprises a field programmable gate array (FPGA).

16. The integrated circuit (IC) of claim 10 wherein the integrated circuit further comprises a programmable logic device (PLD).

17. A method for generating a circuit layout of an integrated circuit (IC), comprising:

obtaining a plurality of column types, wherein each column type of the plurality of column types represents one or more columns in the IC, each column substantially occupied by circuit elements of a circuit type, the one or more columns extending from a side of the IC to an opposite side of the IC;

selecting at least one column type from the plurality of column types; and

forming, at least in part, the circuit layout of the IC using a column associated with the at least one column type.

18. The method of claim 17 wherein the at least one column type is selected from a group consisting of a Configurable Logic Block (CLB) column type, a Multi-Giga Bit Transceiver (MGT) column type, a Block Random Access Memory (BRAM) column type, a Digital Signal Processor (DSP) column type, a multiplier column type, an arithmetic column type, a processor column type, an Input/Output Interconnect (IOI) column type, an Input/Output Block (IOB) column type, and an application specific circuit column type.

19. The method of claim 17 further comprising forming a processor in the circuit layout of the IC.

20. The method of claim 17 further comprising forming configuration logic in a center column positioned on or near a center axis of the IC.

21. A system, using a computer, for laying out a circuit of an integrated circuit (IC), the IC comprising circuitry having programmable functions and programmable interconnects, the system comprising:

means for storing a plurality of column types, wherein each column type of the plurality of column types represents one or more columns in the IC substantially occupied by circuit elements of a circuit type, the one or more columns extending from a side of the IC to an opposite side of the IC;

means for selecting at least two different column types from the plurality of column types; and

means for creating, at least in part, a circuit layout of the IC using columns from the at least two different column types.

22. The system of claim 21 wherein the means for storing includes a database.

23. The system of claim 21 wherein the IC is a field programmable gate array.

24. An integrated circuit (IC) comprising:

a plurality of columns and

wherein each of the columns starts at one side of the IC and ends at an opposite side of the IC,

wherein a first column of the plurality of columns comprises a first set of substantially identical circuit elements of a first circuit type substantially filling the first column,

wherein a second column of the plurality of columns comprises a second set of substantially identical circuit elements of a second circuit type substantially filling the second column, and

wherein a third column of the plurality of columns comprises a third set of substantially identical circuit elements of a third circuit type substantially filling the third column.

25. The integrated circuit of claim 24 further comprising circuitry having programmable functions and programmable interconnects.

26. The integrated circuit of claim 25 wherein the first, second, and third circuit types have a circuit type selected from a group consisting of a Configurable Logic Block (CLB) type, a Multi-Giga Bit Transceiver (MGT) type, a Block Random Access Memory (BRAM) type, a Digital Signal Processor (DSP) circuit type, a multiplier circuit type, an arithmetic circuit type, an Input/Output Interconnect (IOI) circuit

type, an Input/Output Block (IOB) type, and an application specific circuit type.

27. The integrated circuit of claim 26 further comprising a heterogeneous center column having configuration logic, a clock management circuit element, and an input/output block.

28. The integrated circuit of claim 24 wherein the substantially identical circuit elements are substantially identical tiles.

29. The integrated circuit of claim 28 wherein each tile comprises a functional element coupled to a switch matrix.

30. A method for generating a circuit layout of an integrated circuit (IC), the IC comprising circuitry having programmable functions and programmable interconnects, the method comprising:

obtaining a plurality of column types, wherein each column type of the plurality of column types represents one or more columns in the IC, each column substantially occupied by circuit elements of a circuit type, the one or more columns extending from a side of the IC to an opposite side of the IC;

selecting at least three different column types from the plurality of column types; and

forming, at least in part, the circuit layout of the IC using columns from the at least three different column types.

31. The method of claim 30 wherein the selecting at least three different column types is based upon an application area for the IC.

32. The method of claim 31 wherein a column type is selected from a group consisting of a Configurable Logic

Block (CLB) column type, a Multi-Giga Bit Transceiver (MGT) column type, a Block Random Access Memory (BRAM) column type, a Digital Signal Processor (DSP) column type, a multiplier column type, an arithmetic column type, a processor column type, an Input/Output Interconnect (IOI) column type, an Input/Output Block (IOB) column type, an application specific circuit column type, a processor column type having processor elements, a controller column type having controller circuit elements, a graphics column type having graphics circuit, an audio or video column type having audio or video or both circuit elements, a wireless column type having wireless communication elements, a switching column type having switching elements, and a real-time column type having real-time elements.

33. The method of claim 30 wherein the circuit layout of the IC includes an embedded processor.